

FIGURE 1

parameter	meaning	typical value
N	number of input and output ports	64
L	number of input and output lines	512
R	number of lines per port	8
K	number of classes	8
M	number of scheduling modules	16
S	number of pipeline stages per scheduling module	1
C	number of cells per super-cell	8

FIGURE 2

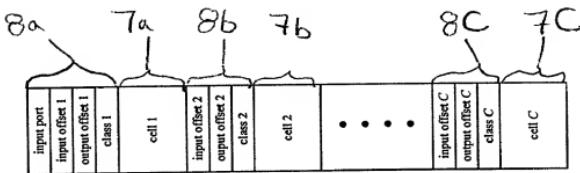


FIGURE 3

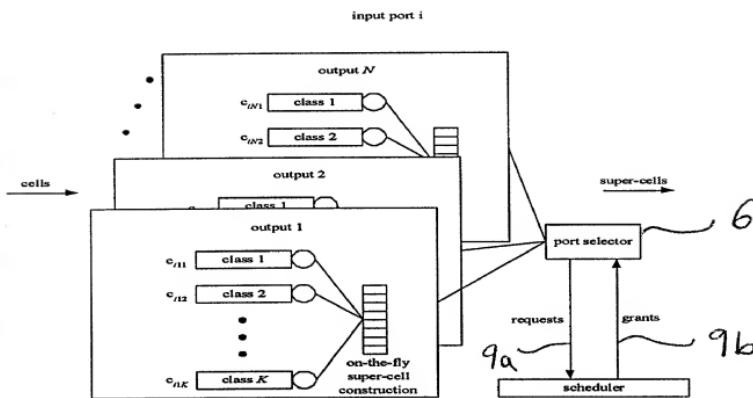


FIGURE 4

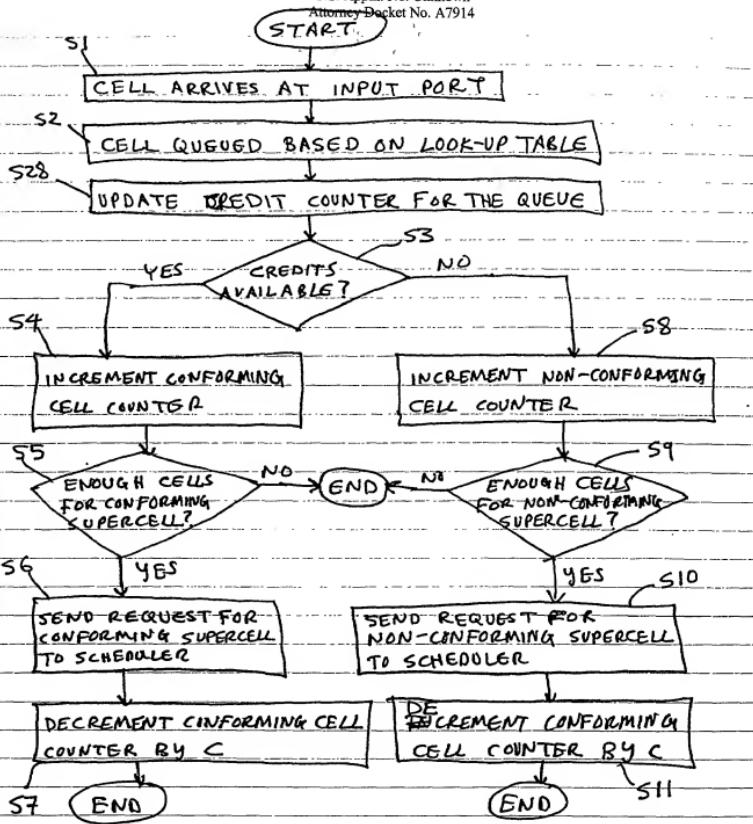


FIGURE 5(a)

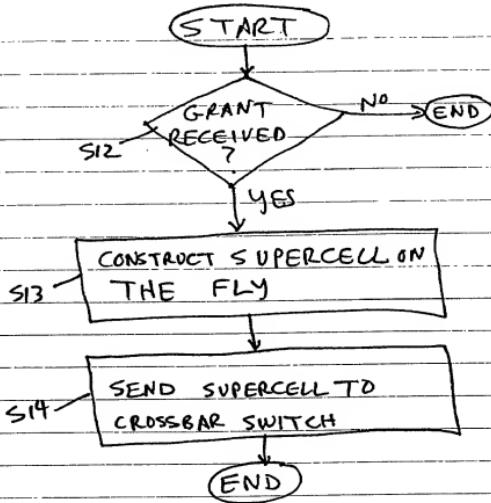


FIGURE 5(b)

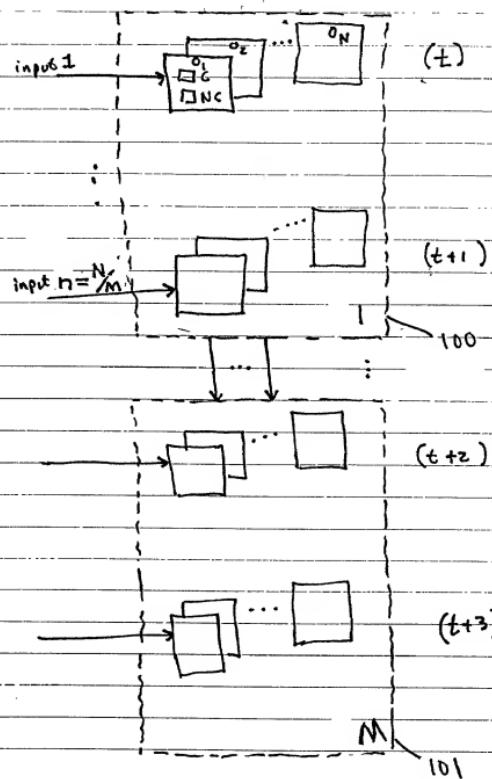


FIGURE 6

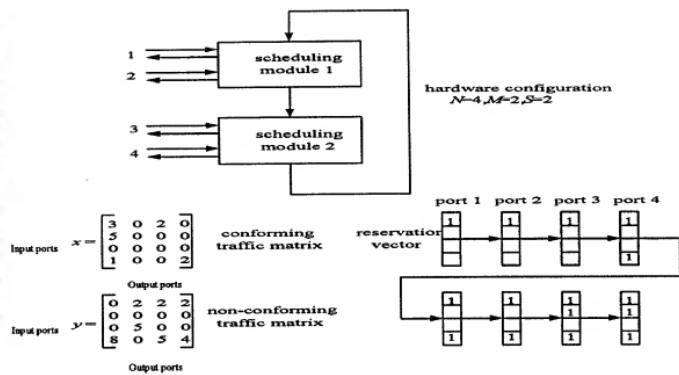
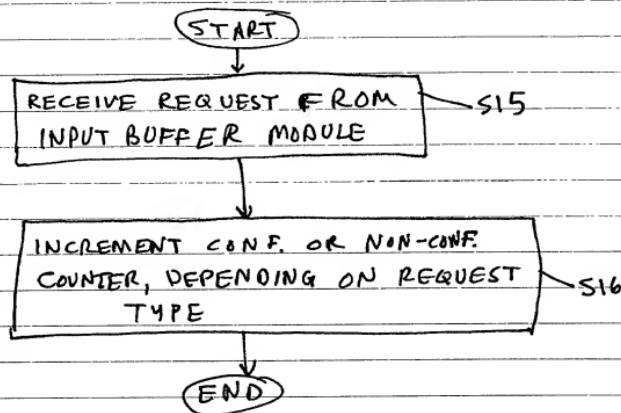


FIGURE 7

FIGURE 8



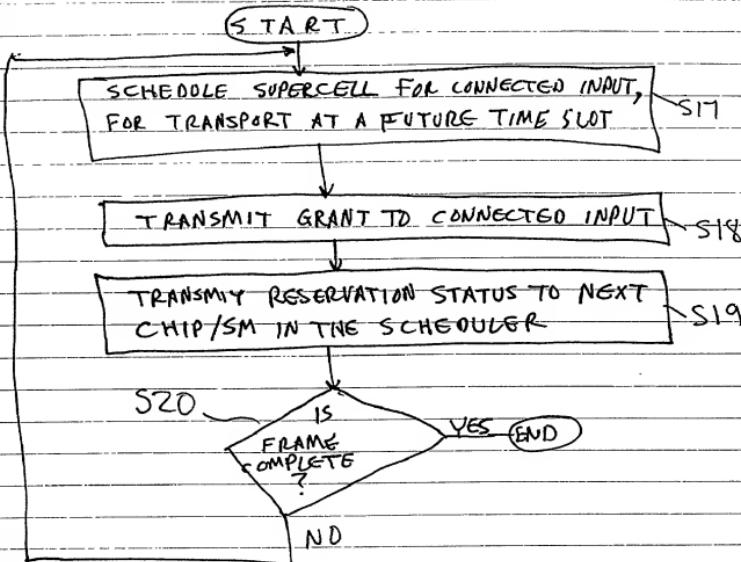


FIGURE 10

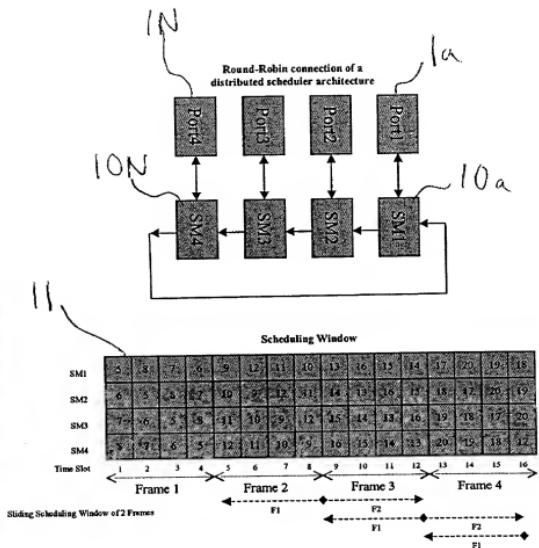


FIGURE . 11

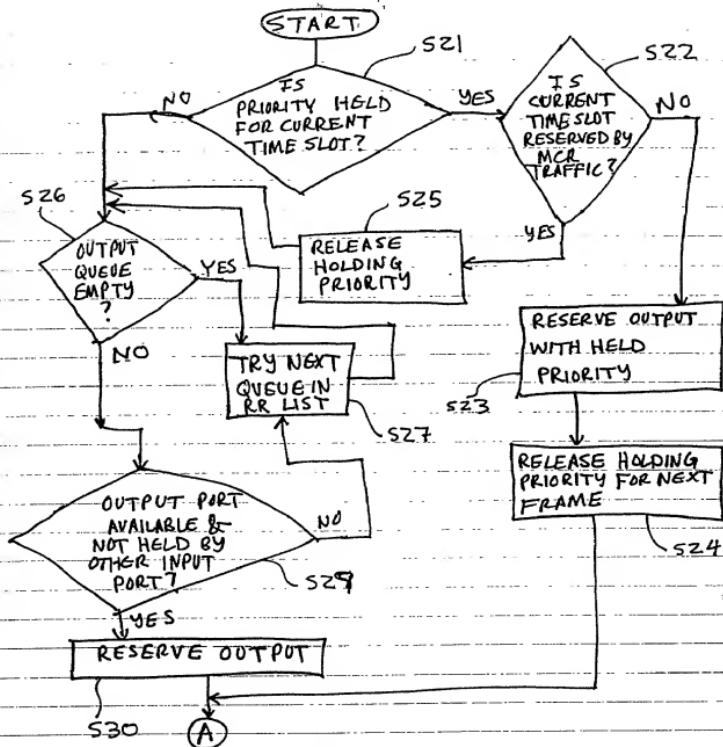


FIGURE 12 (a)

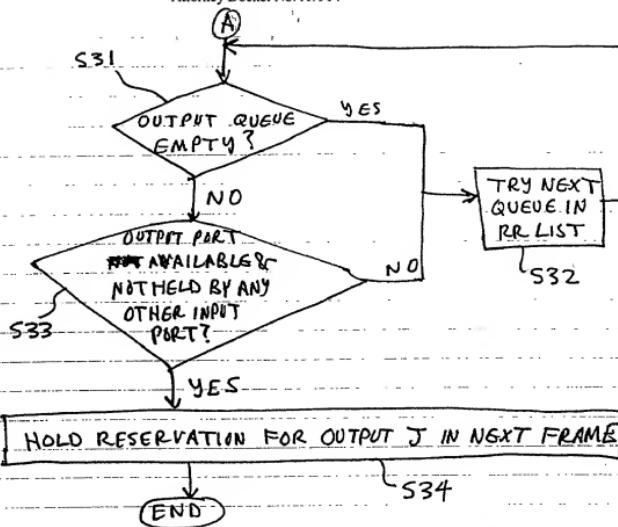


FIGURE 12 (b)

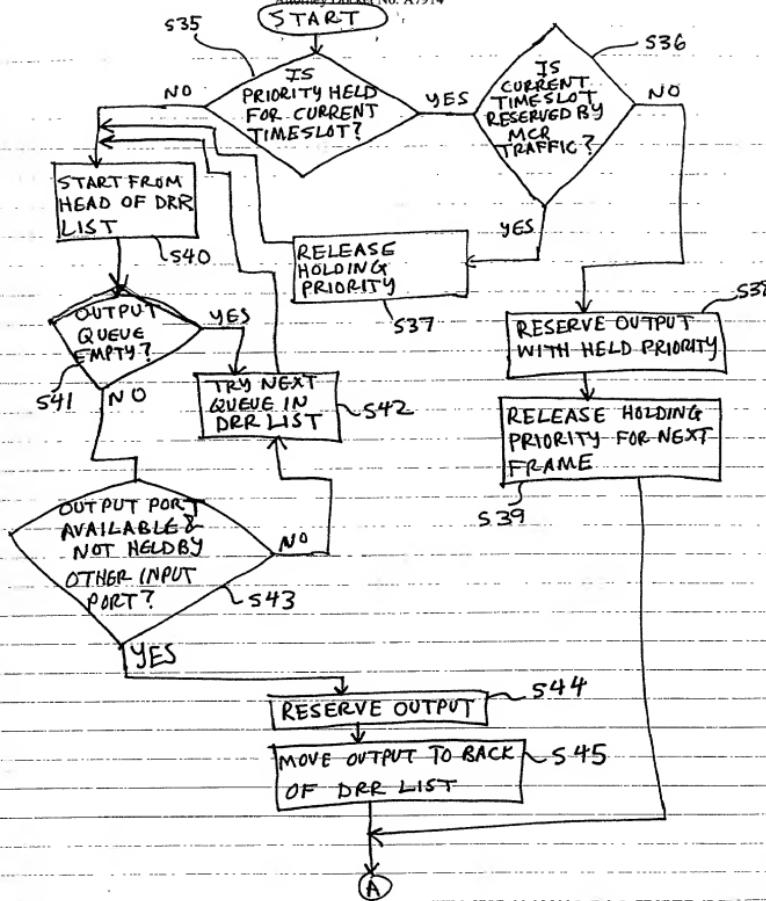


FIGURE 13(a)

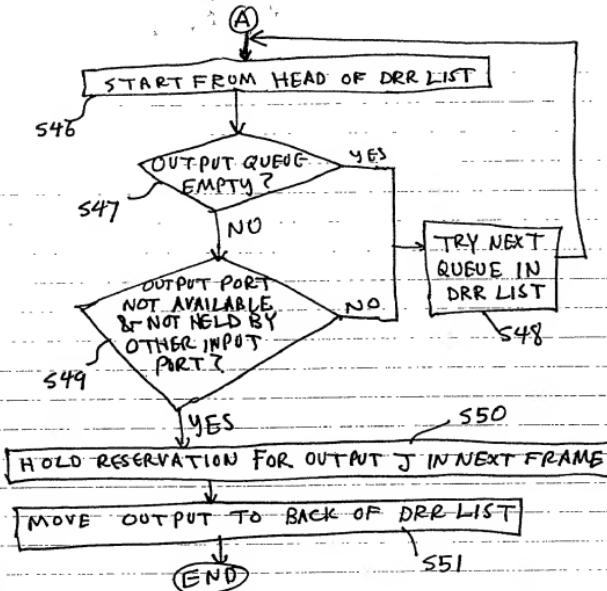


FIGURE 13 (b)

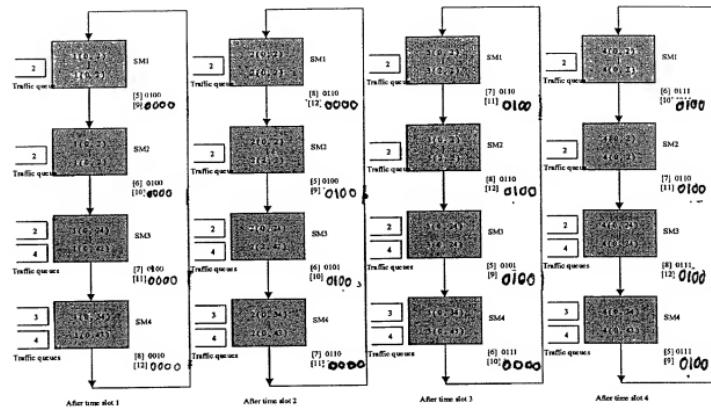


FIGURE 14(a)

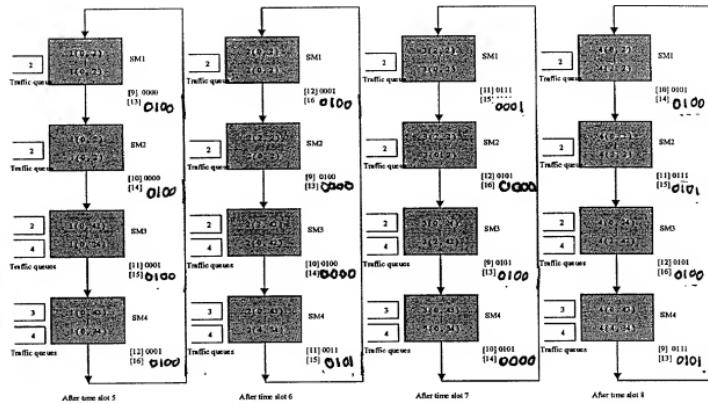


FIGURE 14(b)

Title: Pipeline Scheduler With Fairness and Minimum Bandwidth Guarantee

Inventor: FAN, Ruixue et al.

U.S. Appln. No. Unknown

Attorney Docket No. A7914

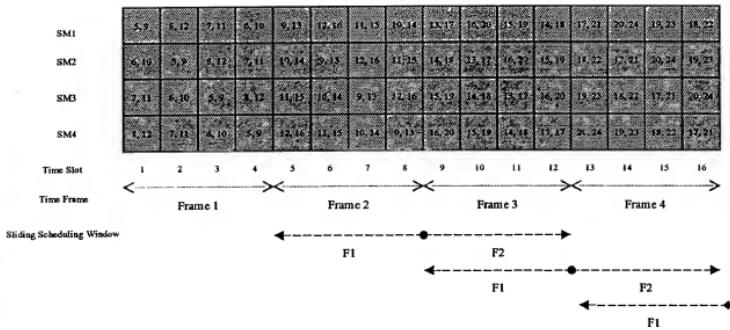
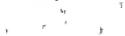


FIGURE 15

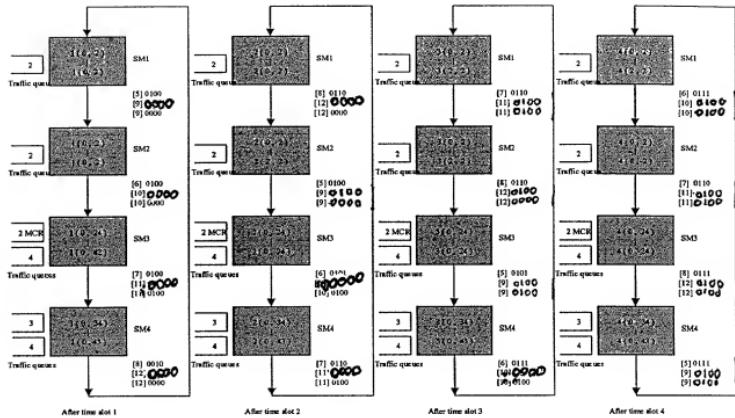


FIGURE 16

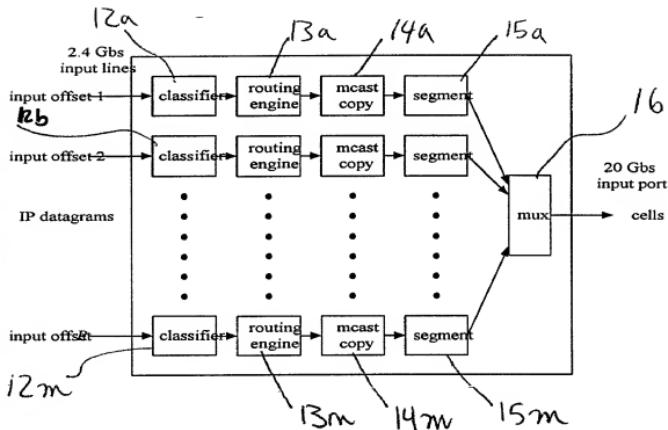


FIGURE 17

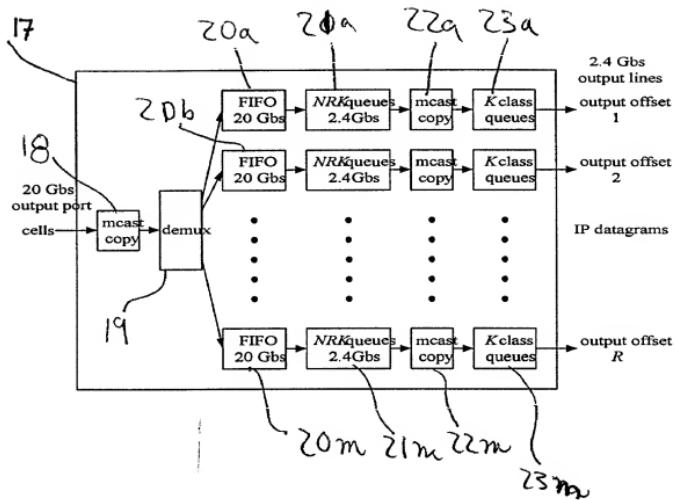


FIGURE 18